Analysis and Design of an E-Band Transformer-Coupled Low-Noise Quadrature VCO in 28 nm CMOS

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***Abstract*—This paper presents an E-Band quadrature voltage-controlled oscillator (QVCO) implemented in 28 nm CMOS. Two fundamental oscillators are coupled by means of gate-to-drain transformers to realize accurate quadrature phases and switched coupled inductors are added for tuning extension. Closed-form expressions of the oscillation frequency and the tuning extension design parameters are derived. The time-variant nature of the circuit-noise to phase-noise of the presented topology is investigated, resulting in simple design guidelines for optimal design. Based on the proposed techniques, the realized prototype is tunable over two bands of almost 5 GHz each separated in frequency, while occupying only 0.031 mm^2. The peak measured phase noise at 10 MHz offset is -117.7 dBc/Hz from a 72.7 GHz carrier and -110 dBc/Hz from a 88.2 GHz carrier and varies less than 3.5 dB within each band.**

***Index Terms*—Quadrature voltage-controlled oscillator (VCO), millimeter-wave (mm-Wave), phase noise, impulse sensitivity function (ISF), transformer, wide tuning range, E-Band, CMOS.**

I. Introduction

The ever increasing demand for higher data-rate and new applications poses unprecedented challenges for wireless systems. CMOS is the technology of choice for mass production digital and is therefore playing a key role in this revolution. Recently, the Federal Communication Commission (FCC) in USA and the European Conference of Postal and Telecommunications Administrations (CEPT) in Europe allocated two bands of 5 GHz each from 71 GHz to 76 GHz and from 81 GHz to 86 GHz (referred as E-Band) to enable high-speed point-to-point wireless link for fiber replacement/extension over short to medium distances [1]. CMOS direct-conversion transceivers stand out for excellent linearity, power and area efficiency also at mm-Wave [2]–[4]. However, this architecture poses serious requirements on the local oscillator (LO), demanding a phase noise (PN) of at least -110 dBc/Hz at 10 MHz offset [2] while providing quadrature (I/Q) outputs directly at the carrier frequency to enable a 16-QAM modulation. Automotive car radar in the frequency band that spans from 77 GHz to 81 GHz, is another application that rises a lot of interest and would benefit from integrated low noise quadrature LO solutions [5].

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The quadrature LO is therefore one of the main bottlenecks that limit the full integration of such radios. To tackle this problem, several solutions have been proposed in literature, but not all of them are suitable for mm-Wave applications, especially when a large tuning range (TR) is required. In [6] a voltage-controlled oscillator (VCO) running at the carrier frequency (f_c) followed by a buffer and a poly-phase filter (PPF) is proposed. The down side of this solution stands in the high insertion loss of the PPF, demanding a power-hungry buffer to drive it. In [7] an injection-locked frequency tripler (ILFM3) is proposed, requiring a VCO that runs at f_c/3 plus a frequency multiplier by 2, a frequency divider by 2, two mixers and two injection-locked VCOs. For such topology a large number of on-chip inductors are needed, resulting in large silicon area and exacerbating the unwanted magnetic coupling from and to other circuits. Moreover, while solutions based on frequency multipliers shows wide tuning range, the work presented by Jani $et\ al.$ in [8] points out that the improvement in terms of phase noise and power consumption is not obvious when the multiplication factor is limited to 2, 3 or 5. Another popular approach is based on coupling two identical oscillators running at f_c to realize a fundamental quadrature VCO. To overcome the well known trade-off between phase noise and phase error of the classical parallel-coupled QVCO [9] a number of alternative techniques have been recently investigated [10]–[14]. Due to the large impact of parasitics at high frequency, a coupling mechanism that does not require extra components is desirable and is therefore adopted in this work.

In [15] we have shown that two fundamental VCOs can be coupled by means of gate-to-drain transformers and switched coupled inductors can be added for tuning extension. The prototype implemented in 28 nm CMOS is tunable over two bands of almost 5 GHz each separated in frequency, while showing state-of-the-art phase noise performance and consuming silicon area of only 0.031 mm^2. In this work a solid theoretical background based on the time-variant nature of circuit-noise to phase-noise conversion [16] is presented. Closed-form expressions of the oscillation frequency and tuning extension design parameters are thoughtfully derived and the effect of tank mismatch over the phase error is investigated, yielding simple design guidelines to minimize phase noise and phase error at the same time. In Section II the proposed transformer-coupled quadrature VCO is presented. The design considerations at mm-Wave and the details of the circuit implementation in deep-scaled 28 nm CMOS are

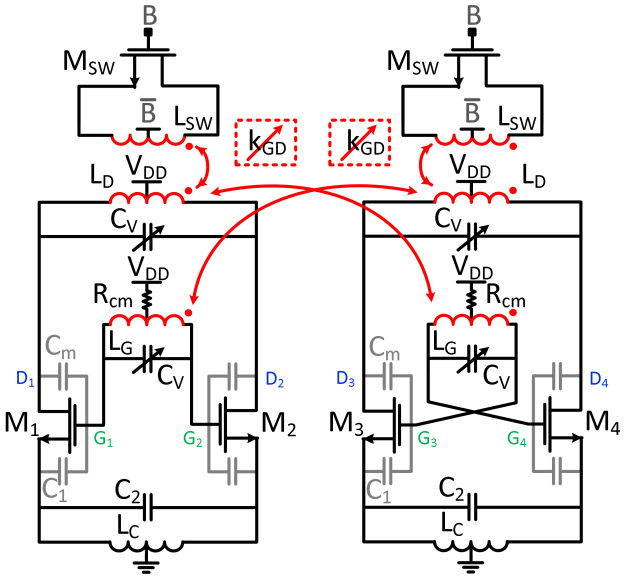

Fig. 1. Schematic of the proposed dual band quadrature VCO based on gate-to-drain transformers with switched coupled inductors.

discussed in Section III. Section IV presents the measured results, demonstrating that the prototype is tunable within two bands separated in frequency and achieves a peak phase noise at 10 MHz offset of -117.7 dBc/Hz from a 72.7 GHz carrier and -110 dBc/Hz from a 88.2 GHz carrier and varies less than 3.5 dB within each band. Conclusions follow in Section V.

II. Proposed Transformer-Coupled Quadrature VCO

A. Operating Principle

Fig.1 shows the schematic of the proposed quadrature oscillator, where two VCOs based on the topology proposed in [17] are coupled by means of two gate-to-drain transformers. To prevent the circuit to oscillate in common mode, a resistor R_{cm} can be added on the low current path through the center tap of L_G as depicted in Fig.1. The LC tank at the source node is designed with a self-resonant frequency lower than the operating frequency of the VCO, it is therefore modeled as an ideal degeneration capacitor C_2 in parallel with a RF choke inductor L_C. To gain insight into the principle of operation and simplify the following analysis, it is functional to replace the resonator with its single-ended two-port admittance parameters model as in Fig.2, where C_D=2C_V, L_0=L_G/2=L_D/2 and R_p accounts for the losses. By inspection, the following equations are derived:

$$Y_{11} = Y_{22} = \frac{1}{R_p} + sC_D + \frac{1}{sL_0(1-k_{GD}^2)} \tag{1}$$

$$Y_{12} = Y_{21} = \frac{k_{GD}}{sL_0(1-k_{GD}^2)} \tag{2}$$

In steady state due to the large signal operation, the non linearity of the active device and the pass-band behavior of the tank, it is possible to replace the transconductor with its

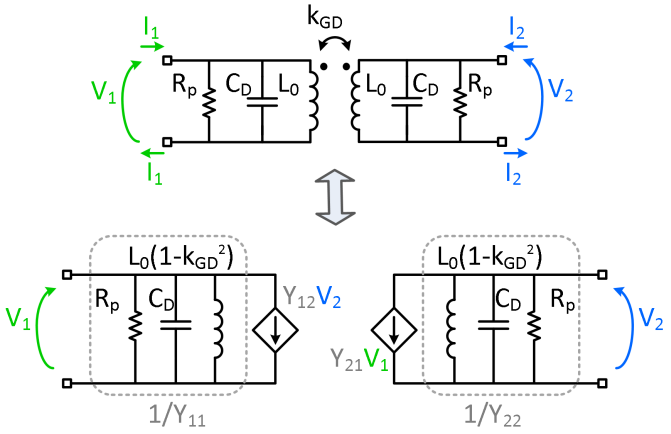

Fig. 2. Lumped element model of the proposed resonator and equivalent circuit based on the two-port admittance parameters matrix.

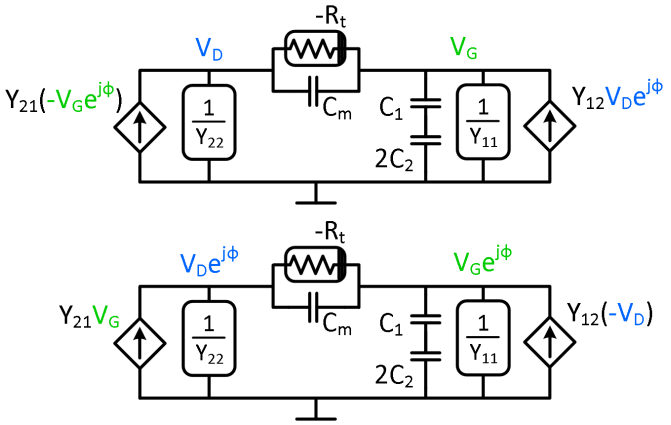

Fig. 3. Single-ended half circuit negative resistance AC model of the proposed QVCO.

describing function approximation [18]. By means of a Norton transformation and assuming differential operation (i.e. $V_{D1} = -V_{D2} = V_D$, $V_{D3} = -V_{D4} = V_D e^{j\phi}$, $V_{G1} = -V_{G2} = V_G$ and $V_{G3} = -V_{G4} = V_G e^{j\phi}$) it is possible to redraw the circuit in Fig.1 as in Fig.3 (see Appendix for further details). From Kirchhoff's phasor nodal equations, the following expressions are derived:

$$V_D = V_G \cdot \frac{-Y_{21}e^{j\phi} + sC_m - 1/R_t}{Y_{22} + sC_m - 1/R_t} \tag{3}$$

$$V_D e^{j\phi} = V_G \cdot \frac{Y_{21} + e^{j\phi}(sC_m - 1/R_t)}{Y_{22} + sC_m - 1/R_t} \tag{4}$$

This set of equations is verified if and only if ϕ=$\pm\pi$/2. Meaning that in presence of perfectly matched components the two oscillators are forced to operate in quadrature. Furthermore, a perfect quadrature operation is realized even if $Y_{11} \neq Y_{22}$.

B. Oscillation Frequency

To derive a closed-form expression for the oscillation frequency, it is effective to rearrange the circuit as a tank of

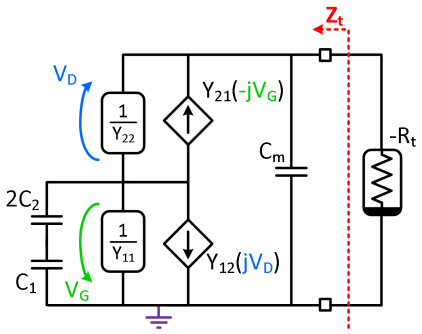

Fig. 4. Rearrangement of the circuit in Fig.3 under quadrature operation.

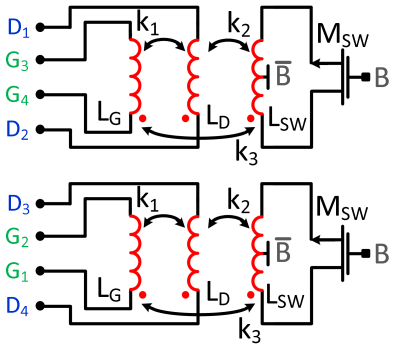

Fig. 5. Simplified lumped element model of the gate-to-drain transformers with switched coupled inductors.

impedance Z_t in parallel with an energy restoring element $-R_t$. By noting that the oscillator operates in quadrature, the circuit in Fig.3 can be redrawn as shown in Fig.4. By inspection, Z_t is derived as in (5). Assuming a high quality factor for the resonator ($Rp \rightarrow +\infty$) and imposing the condition $Den\{Z_t\} = 0$, the two resonant frequencies of the 4th order tank are derived as

$$\omega_{1,2}^2 = \frac{2 + \alpha_1 \pm \sqrt{\alpha_2^2 + 4k_{GD}^2(\alpha_1 + \alpha_3) + 4}}{2L_0C_m(1 - k_{GD}^2)(\alpha_1 + \alpha_3)} \tag{6}$$

where $\alpha_1 = (C_D + C_G)/C_m$, $\alpha_2 = (C_D - C_G)/C_m$, $\alpha_3 = C_DC_G/C_m^2$ and $C_G = C_D + C_1 2C_2/(C_1 + 2C_2)$.

Noteworthy, this expression is similar to the one derived in [12] being the two quadrature VCOs realized around similar 4th order tanks (here C_m plays a role similar to C_C in [12]). Moreover, in principle it is possible to use the second mode of oscillation to extend further the tuning range, provided that extra circuitry is added as already proposed for other oscillator topologies [12], [19], [20]. However, given the high target frequency of operation, in this work no effort is made to take advantage of the second resonance peak, since adding extra components would lead to higher parasitic loading of the tank. Nevertheless, during the design phase it is important to ensure that the oscillator meets the Barkhausen's criteria only in one mode. Condition easily achieved in a practical design at mm-Wave frequencies when the magnetic coupling k_{GD} is designed large enough, so that $\omega_2 \gg \omega_1$ and the transconductors are not able to compensate for the tank losses in the second mode.

C. Tuning Extension

In LC oscillators higher tuning range comes at the cost of lower spectral purity for a given power consumption. This trade-off is exacerbated at mm-Wave, where the impact of parasitics is larger and the quality factor of the tank is limited by the Q of capacitors and varactors rather than the one of inductors. For these reasons, several recent research works have been focused on alternative tuning extension techniques [21]–[23].

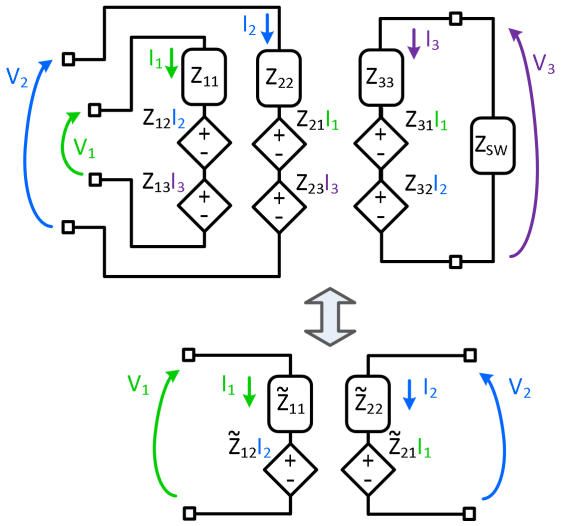

Fig. 6. Transformer with switched coupled inductor three-port impedance parameters model (top) and its two-port equivalent circuit (bottom).

From (6) it is clear that the oscillation frequency is highly sensitive to the magnetic coupling coefficient k_{GD} and the inductance value L_0. In this work, a third winding L_{SW} terminated on a switch M_{SW} is coupled to the gate-to-drain transformer to effectively change both k_{GD} and L_0, as depicted in Fig.5. Intuitively, when the switch is turned ON, the current induced in L_{SW} through k_2 and k_3 finds a low impedance path. Whereas, when M_{SW} is in OFF state, L_{SW} is terminated on an infinite impedance and ideally no

$$Z_t = \frac{j\omega L_0\left[(k_{GD}^2 - 1)L_0\omega^2 + 2 - j\frac{2(k_{GD}^2 - 1)L_0\omega}{Rp}\right]}{-\omega^4 L_0^2(k_{GD}^2 - 1)[(C_G + C_m)C_D + C_GC_m] + j\frac{(k_{GD}^2 - 1)(C_D + C_G + 2C_m)L_0^2\omega^3}{R_p} + \omega^2\left[\frac{(k_{GD}^2 - 1)L_0^2}{R_p^2} - (C_D + C_G + 2C_m)L_0\right] + j\frac{2L_0\omega}{R_p} + 1} \tag{5}$$

current is flowing. To gain deeper insight into the operation of the proposed transformer with switched coupled inductor and derive design guidelines, it is useful to refer to its three-port impedance parameter model shown in Fig.6. By inspection the following expression are derived

$$Z_{11} = R_G + sL_G \tag{7}$$

$$Z_{22} = R_D + sL_D \tag{8}$$

$$Z_{33} = R_{SW} + sL_{SW} \tag{9}$$

$$Z_{12} = Z_{21} = sk_1\sqrt{L_G L_D} \tag{10}$$

$$Z_{23} = Z_{32} = sk_2\sqrt{L_D L_{SW}} \tag{11}$$

$$Z_{13} = Z_{31} = sk_3\sqrt{L_G L_{SW}} \tag{12}$$

where the losses of each inductor (L_G, L_D and L_{SW}) in Fig.5 are modelled by a series resistor (of value R_G, R_D and R_{SW} respectively).

Since the third port is terminated on an impedance Z_{SW}, it is possible to derive the equivalent two-port network as depiced in Fig.6, provided that

$$\widetilde{Z}_{11} = Z_{11} - \frac{Z_{13}Z_{31}}{Z_{SW} + Z_{33}} \tag{13}$$

$$\widetilde{Z}_{12} = Z_{12} - \frac{Z_{13}Z_{32}}{Z_{SW} + Z_{33}} \tag{14}$$

where for sake of space only the expressions for the impedance and the transimpedance of the first winding are reported.

It is now possible to derive approximated equations to describe an equivalent two-port transformer. When M_{SW} is in ON state $Z_{SW} \approx R_{ON}$ and assuming $R_{SW}+R_{ON} \ll \omega L_{SW}$, the equivalent series resistance and self-inductance of the primary winding ($R_{G,ON}$, $L_{G,ON}$) and the equivalent magnetic coupling $k_{GD,ON}$ are

$$R_{G,ON} \approx R_G + k_3^2\frac{L_G}{L_{SW}}(R_{SW} + R_{ON}) \tag{15}$$

$$L_{G,ON} \approx L_G - L_G k_3^2 \tag{16}$$

$$k_{GD,ON} \approx \frac{k_1 - k_2 k_3}{\sqrt{(1-k_2^2)(1-k_3^2)}} \tag{17}$$

When M_{SW} is in OFF state $Z_{SW} \approx 1/(sC_{OFF})$ and assuming $R_{SW}^2 \ll (\omega L_{SW} - 1/(\omega C_{OFF}))^2$, the following expressions are derived

$$R_{G,OFF} \approx R_G + \frac{k_3^2}{(\omega_{SW}^2/\omega^2 - 1)^2}\frac{L_G}{L_{SW}}R_{SW} \tag{18}$$

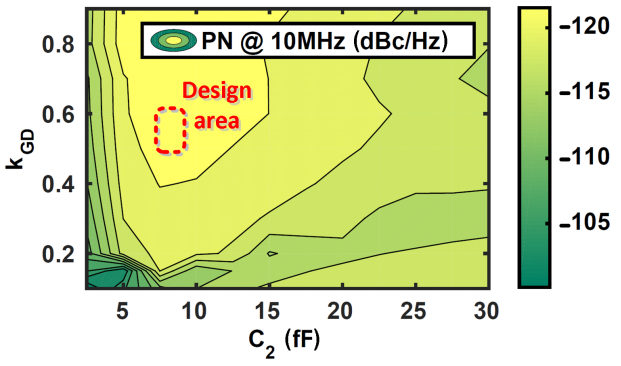

Fig. 7. Simulated phase noise at 10 MHz offset from an 80 GHz carrier versus k_{GD} and C_2.

$$L_{G,OFF} \approx L_G + L_G\frac{k_3^2}{\omega_{SW}^2/\omega^2 - 1} \tag{19}$$

$$k_{GD,OFF} \approx \frac{k_1 + \dfrac{k_2 k_3}{(\omega_{SW}^2/\omega^2 - 1)}}{\sqrt{\left[1 + \dfrac{k_2^2}{\omega_{SW}^2/\omega^2 - 1}\right]\left[1 + \dfrac{k_3^2}{\omega_{SW}^2/\omega^2 - 1}\right]}} \tag{20}$$

where $\omega_{SW}^2 = 1/(L_{SW}C_{OFF})$ is the self-resonance frequency of the third winding when terminated on the OFF capacitance of M_{SW}.

From (15), (16), (17), (18), (19) and (20) several design considerations can be made. Fist, the ON resistance of M_{SW} severely limits the transformer losses and should be designed accordingly low enough. In addition, the current induced in the third winding effectively reduces both $L_{G,ON}$ and $k_{GD,ON}$ through k_2 and k_3.

Another critical observation deals with the design of ω_{SW} when M_{SW} is in OFF state. To ensure a single solution of equation (19), ω_{SW} should be higher than the oscillation frequency ω_o of the VCO, imposing an upper bound for the value of C_{OFF} [21], [23]. Moreover, in a practical design, the condition $\omega_{SW} \gg \omega_o$ is not verified. Meaning that $R_{G,OFF}$, $L_{G,OFF}$ and $k_{GD,OFF}$ increase with frequency and the change is sharper when ω_o approaches ω_{SW}, demanding for a careful co-design of M_{SW}, L_{SW}, k_2 and k_3.

D. Phase Noise

The first step towards a design for minimum phase noise is to quantify the effect of two key design parameters (i.e. the equivalent magnetic coupling k_{GD} and the degeneration capacitance C_2) on the operation of the proposed quadrature oscillator. Fig.7 shows the simulated phase noise at 10 MHz offset from an 80 GHz carrier as a function of k_{GD} and C_2. The experiments were performed adopting ideal lumped element components for passive devices where $C_V = 10fF$, L_0 is adjusted to keep the oscillation frequency equal to 80 GHz for fair comparison and the losses are modelled with a shunt resistor assuming a quality factor equal to 4. The transconductors (W/L of 40 μm/28 nm) were post-layout

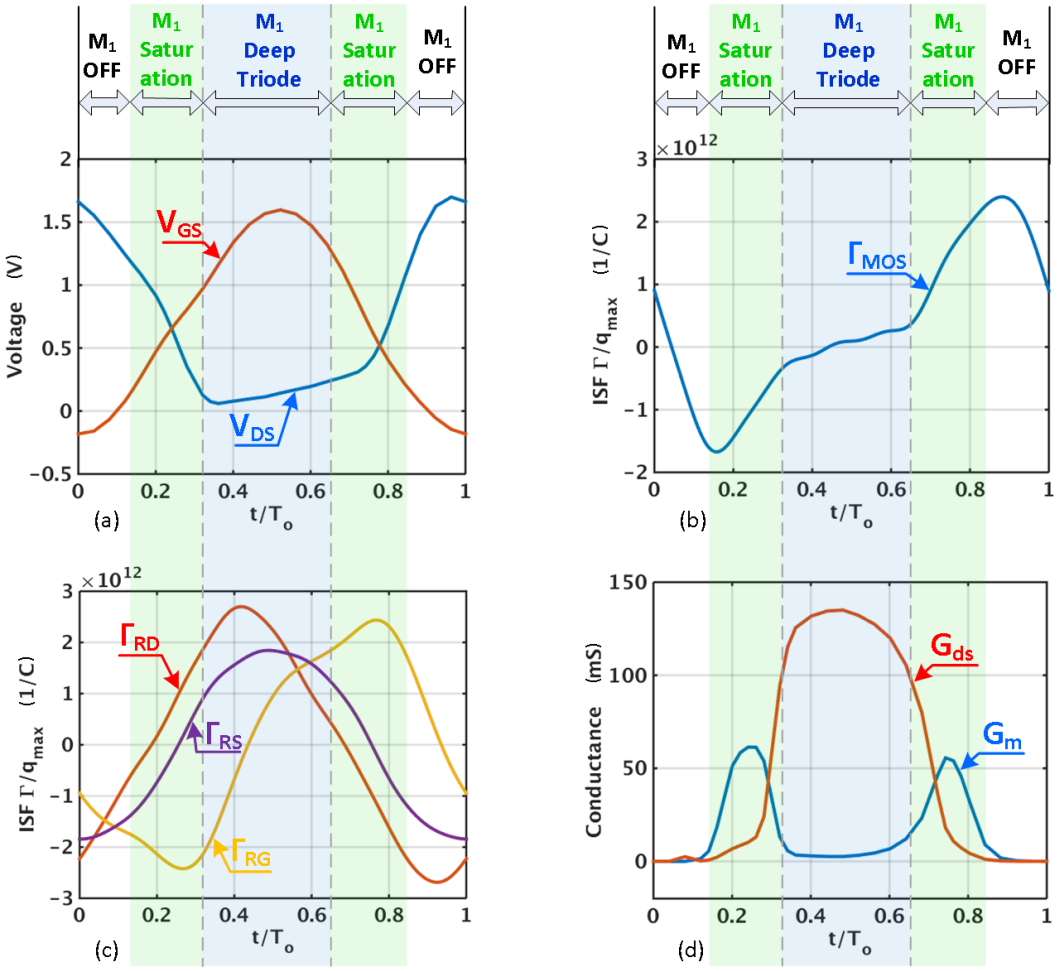

Fig. 8. Noise to phase noise conversion mechanism of the proposed oscillator. (a) Voltage waveforms and M_1 operation region. (b) Impulse sensitivity function of M_1 channel noise. (c) Impulse sensitivity function at different nodes. (d) Instantaneous transconductance (G_m) and channel conductance (G_{ds}) of M_1.

parasitic extracted to account for C_m and C_1 (about 10 fF and 20 fF respectively). R_{cm} is set to 100 Ω to prevent oscillation in common mode. Clearly, the phase noise shows a weak dependency from k_{GD}, meaning that the proposed tuning extension technique can be effectively applied provided that the quality factor of the resonator is kept constant when M_{SW} is in ON and OFF state. Moreover, the value of C_2 can be optimized for PN.

To get deeper insight into the circuit-noise to phase-noise conversion mechanism of the proposed topology it is useful to adopt the linear time-variant approach proposed by Hajimiri and Lee in [16]. By noting that in steady state the oscillation amplitude is limited by the compressing behavior of the transconductors, the amplitude noise is neglected and the phase noise at an angular frequency offset $\Delta\omega$ from a ω_o carrier can be expressed as

$$L(\Delta\omega) = 10log_{10}\left(\frac{\sum_i N_{L,i}}{2q_{max}^2(\Delta\omega)^2}\right) \tag{21}$$

where q_{max} is the maximum charge displacement across the tank capacitor and $N_{L,i}$ is the effective noise power of the i-th current noise source, defined as

$$N_{L,i} = \frac{1}{T_o}\int_0^{T_o} \Gamma_i^2(t)\ \overline{i_{n,i}^2(t)}\ dt \tag{22}$$

where $\Gamma_i(t)$ is the impulse sensitivity function (ISF), dimensionless function of time periodic in $T_o = 2\pi/\omega_o$ and $\overline{i_{n,i}^2}$ is the power spectral density of the current noise produced by the i-th devices.

The ratio $\Gamma_i(t)/q_{max}$ is accurately estimated at different oscillator nodes by means of the periodic transfer function analysis (PXF) as proposed in [24] and reported in Fig.8(c). In these experiments $k_{GD} = 0.5$ and the optimum value of C_2 in Fig.7 is selected. Most importantly, Fig.8(c) shows that $\Gamma_{RS,rms}^2 \approx 0.65\ \Gamma_{RG,rms}^2 \approx 0.54\ \Gamma_{RD,rms}^2$, meaning that the source node is the less sensitive to noise and the drain node is the most critical one. To optimize the phase noise performance is therefore important to design the transformer accordingly (i.e. the quality factor of the secondary winding Q_D should be maximized). Moreover, the output should be probed at the source to minimize the loading effect of the following stage.

Fig.8(a) shows the voltage waveforms across M_1 highlighting its regime of operation. Due to the large voltage amplitude

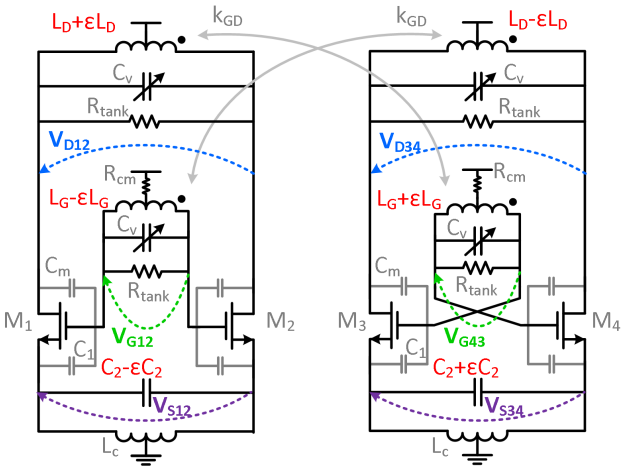

Fig. 9. Test circuit to evaluate the phase error in presence of mismatch.

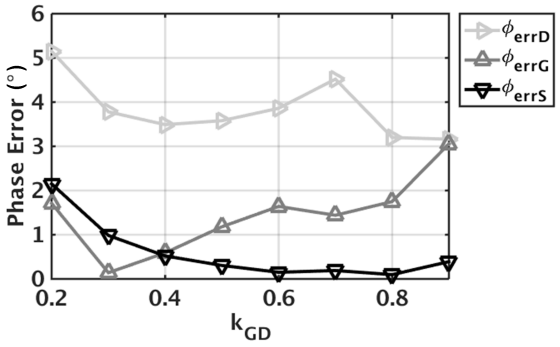

Fig. 10. Simulated impact of 2ε=2% mismatch among passives on the phase error at different nodes against k_{GD}.

the transistor operates in all three regions (i.e. saturation, triode and OFF), meaning that the active device 1) contributes to losses through the channel conductance G_{ds} (referred in literature as loaded or effective Q-factor [25], [26]) and 2) injects more noise through G_{ds} and the larger required G_m. Although in theory this condition is not desirable, in mm-Wave oscillators realizing a high common mode impedance at $2f_o$ over the whole tuning range is not trivial [27], and the transconductors are allowed to ender (to some extend) the triode region to maximize the voltage amplitude. The noise contribution of the transistor can be expressed as [25]

$$\overline{i^2_{n,MOS}(t)} = 4K_BT(\gamma G_m(t) + G_{ds}(t)) \tag{23}$$

where K_B is the Boltzmann's constant, T absolute temperature and γ the transistor channel noise factor.

Noteworthy, Fig.8(b),(d) show that when the transistor noise contribution is at its maximum, the associated Γ_{MOS} is close to 0 yielding a negligible associated effective noise power $N_{L,MOS} \approx 0$ during this laps of time.

E. Phase Error

In presence of mismatches in the circuit equations (3) and (4) are not valid anymore and the two oscillators depart from quadrature. This result in amplitude imbalance and phase error. The focus of this Section is the phase error, since in a practical system the LO signals are normally fed to hard limiting buffers and an I/Q mixer that is almost insensitive to small amplitude imbalance (provided that the signal amplitude is large) [9], [11]. Deriving elegant closed-form expressions for the phase error at different tank nodes under the presence of mismatches for this QVCO topology is not trivial. Moreover, the simplified linear model in Fig.3 when extended to describe mismatch due to the tank, would not account for circuit nonlinearity that may play a significant role (as is the case for QVCO that employs passive nonlinear coupler [11]).

To address this problem, it is functional to refer to the schematic depicted in Fig.9. To gain a deeper understanding, a mismatch of $2\varepsilon = 2\%$ is imposed among passives and the phase error is evaluated at different nodes. Fig.10 shows that when the equivalent magnetic coupling is $k_{GD} > 0.3$ the phase error at the source node is always $\phi_{errS} \leq 1°$ and most importantly when $k_{GD} > 0.4$ the condition $\phi_{errS} \leq \phi_{errG} \leq \phi_{errD}$ is achieved.

From the analysis above, we can draw two very important and perhaps unexpected conclusions, 1) probing the signal at the source leads to the same choice of optimal design parameters for both minimum phase noise (as in Fig.7) and minimum phase error (Fig.10), and 2) the loading effect of the buffer is minimal at this node (as clear from Fig.8(c) and already discussed in Section II-D).

III. Design Considerations at mm-Wave and Circuit Implementation

Thanks to the aggressive scaling of the gate length, nowadays mm-Wave circuits can enjoy active devices with a f_t as high as 300 GHz in technology nodes as 28 nm CMOS [28]. However, when these transconductors with high intrinsic performance are used in LC oscillators the effect of the parasitics due to the layout interconnects severely limits the improvement in terms of effective f_t and yields large fixed capacitance making the tuning range vs. phase noise trade-off tighter [29]. Furthermore, in deep-scaled CMOS processes 1) low level metals get thinner and closer to the substrate, reducing the quality factor of metal-oxide-metal (MOM) capacitors, 2) high level metals get closer to the substrate, lowering the achievable Q of inductors and 3) the design rule check (DRC) imposes ever increasing minimum metal density to be fulfilled in tighter area windows, limiting even further the maximum achievable Q-factor and self-resonance frequency of on-chip inductors [22], [30]. A number of design techniques are discussed in this Section to tackle the aforementioned challenges for mm-Wave LC oscillators.

As a first step, we focus on the design and layout of the active core. The parasitic gate-to-drain capacitance plays an important role in the design of any LC oscillator, lowering the oscillation frequency and limiting the tuning range [31], and the presented topology is no exception. As a matter of fact, C_m shown in Fig.1 appears single-ended, lowering the oscillation frequency as clear from (6). This capacitance is kept minimum by adopting the transistor layout presented in [29] and shown

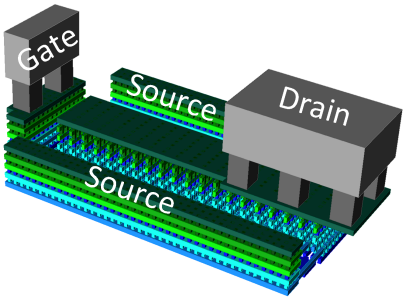

Fig. 11. 3-D layout view of the designed transistor M_1 40 μm/28 nm.

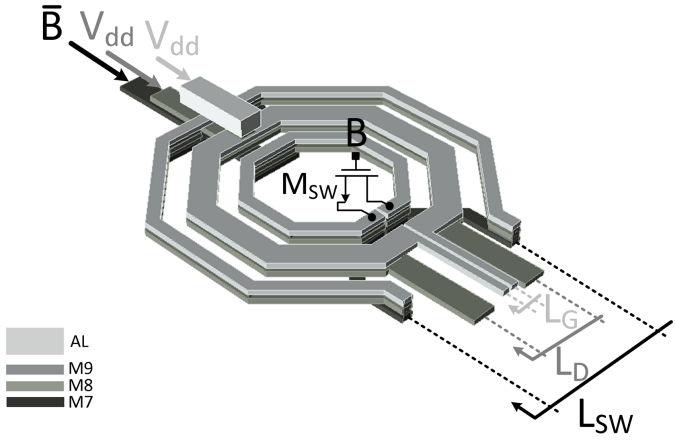

Fig. 12. 3-D layout view of the designed transformer with switched coupled inductor.

in Fig.11. Moreover, thanks to this layout, it is now possible to access directly the gate and drain of the transistor in higher metal, limiting the losses due to interconnections to the tank. The source node is accessed at both sides, minimizing the critical gain reduction due to the connection to this net and simplifying the routing to C_2 and L_C shown in Fig.1. In this design, the trasistors are oversized to 40 μm/28 nm to account for possible model inaccuracy.

Another key aspect of any mm-Wave LC oscillator is the design and layout of the tank. Fig.12 shows the 3-D view of the layout of the proposed gate-to-drain transformer. A relatively high value of the magnetic coupling coefficient between the primary and secondary windings k_1 (see Fig.5) is desirable, so that it becomes the dominant factor in the expressions of equivalent magnetic coupling k_{GD} in ON and OFF state (17), (20). Since the value of the required self-inductances is relatively low, to maximize the magnetic coupling L_G and L_D are realized as an overlay transformer in metal 9 and 8 respectively (see Fig.12), with a metal width of 4 μm and an outer diameter of 37.8 μm.

The switched coupled inductor L_{SW} in Fig.5 is realized with an inner coil and an outer coil in both metal 8 and 9 with 2 μm width, connected together in metal 7. The inner and outer spacing of L_{SW} from the primary and secondary windings (i.e. L_G and L_D) are 2.9 μm and 3.5 μm respectively (as shown in Fig.12). As discussed in Section II-C the value of R_{ON} and C_{OFF} of the switch M_{SW} proves critical. Since at mm-Wave the inductor Q-factor is relatively high, the value

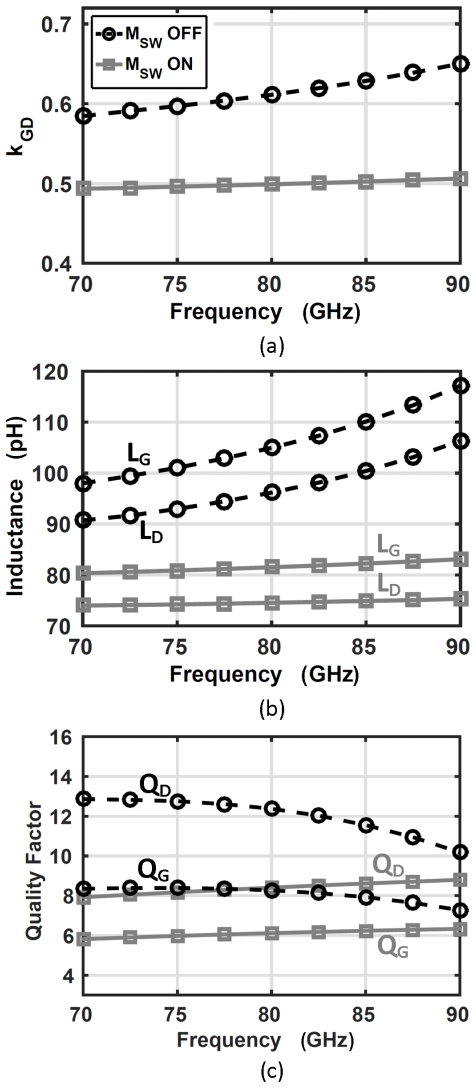

Fig. 13. Simulated characteristics of the gate-to-drain transformer with switched coupled inductor when M_{SW} is ON (solid grey line) and OFF (dashed black line) against frequency. (a) Equivalent magnetic coupling k_{GD}. (b) Self-inductance of the primary and secondary winding (L_G and L_D). (c) Quality factor of the primary and secondary winding (Q_G and Q_D).

of R_{ON} will dominate the losses of the transformer in the ON state, as predicted from (15). M_{SW} is therefore designed large, with a W/L of (39x3) μm/28 nm. To further optimize the switch Figure of Merit (FOM$_{SW}$ = $R_{ON}C_{OFF}$), the source and drain connections of M_{SW} are layouted with a tapered via stack to minimize C_{OFF}. Fig.13 shows the proposed gate-to-drain transformer with switched coupled inductor simulated parameters when the switch is in ON and OFF state. From electromagnetic simulation the equivalent magnetic coupling coefficient (Fig.13(a)), self-inductances (Fig.13(b)) and quality factors (Fig.13(c)) of primary and secondary windings of the transformer when M_{SW} is OFF (ON) are k_{GD}=0.59 (0.5), L_G=100 pH (82 pH), L_D=92 pH (75 pH), Q_G=8 (6), Q_D=13 (9) at 73.5 GHz (83.5 GHz). It is worth to mention that, as clear from the discussion about circuit-noise to phase-noise conversion in Section II-D and shown in Fig.13(c), the winding with the higher quality factor is reserved to L_D.

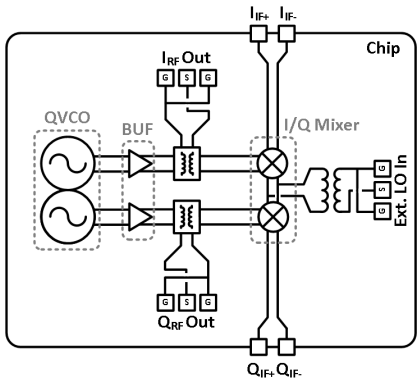

Fig. 14. Block diagram of the realized test chip.

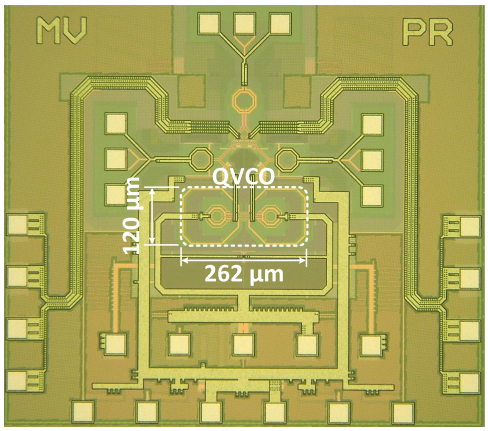

Fig. 15. Die micrograph of the realized test chip (core dimensions: 120 μm x 262 μm).

To compensate for the degradation of the tank Q in the higher band (i.e. when M_{SW} is in ON state), in this work the value of the degeneration capacitance C_2 is designed for optimal phase noise in this mode of operation, aiming at an uniform noise FOM over the whole tuning range. To further tune the oscillator continuously within the two bands, 2 binary-weighted digitally controlled MOM capacitors and an accumulation-mode MOS (A-MOS) varactor are added to the tank.

To minimize the flicker noise to phase noise up-conversion, a voltage-biased topology is adopted in this design. Removing the current control is a critical choice, common to several state-of-the-art low-noise mm-Wave LC oscillators (such as [13], [22], [27], [32]). In fact, the lack of ideal current sources is exacerbated at high frequencies by the larger effect of the parasitic capacitance to the substrate.

Fig.14 shows the block diagram of the realized chip. For measurement purpose, two buffers and an I/Q double-balanced mixer are also implemented on-chip. The buffers are realized with pseudo-differential neutralized common source amplifiers, providing high input-output isolation, driving the 50 Ω measurement equipment directly at mm-Wave and controlling the on-chip mixer. The latter is based on a Gilbert cell, allowing the downconversion of the high frequency on-chip quadrature signals to an intermediate frequency, instrumental to measure I/Q amplitude and phase imbalance.

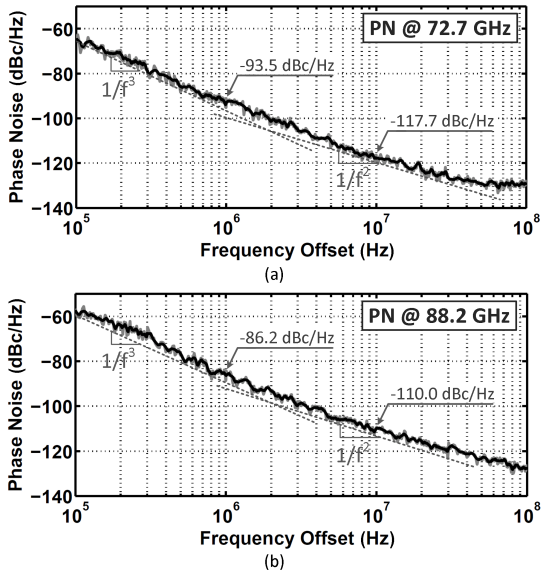

Fig. 16. Measured phase noise from a 72.7 GHz carrier (a) and from a 88.2 GHz carrier (b).

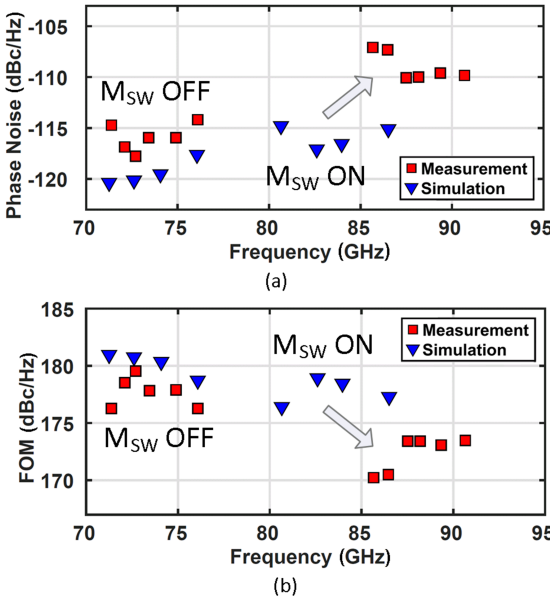

Fig. 17. Measured and simulated phase noise (a) and noise FOM (b) at 10MHz offset from the carrier against frequency.

IV. Measurement Results

Fig.15 shows the die micrograph of the quadrature VCO prototype fabricated in 28 nm bulk CMOS technology with no RF thick metal option. It occupies an active area of only 0.031 mm^2. All the measurements are performed on a high frequency probe station. The mm-Wave output of the QVCO after the buffer and the external LO input of the double balanced I/Q mixer (see Fig.14) are directly accessed by GSG probes, while the dc and IF signal pads are wire-bonded to a printed circuit board (PCB). The quadrature VCO consumes 35.6 mW from a 0.7 V supply. The oscillation frequency is tunable from 71.4 GHz to 76.1 GHz when M_{SW} is OFF and from 85.6 GHz to 90.7 GHz when M_{SW} is ON, corresponding to 9.8 GHz

TABLE I
COMPARISON WITH STATE-OF-THE-ART INTEGRATED QUADRATURE FREQUENCY GENERATION CIRCUITS IN THE 70/100 GHZ BAND

	Topology	Frequency (GHz)	TR (GHz)	Power (mW)	PN@10 MHz (dBc/Hz)	FOM (dBc/Hz)	FOM_A (dBc/Hz)	Phase Error	Area (mm^2)	Technology
[6]	VCO + RC PPF	70-89	19	310.2	-107/-114(1)	159/168.1	168.7/177.8	<8.5°	0.107(2)	0.35 μm SiGe
[7]	ILFM3	70.5-85.5	15	47.3	-111.7/-115.8(1)	173.5/176.3	178.9/181.7	<2°	0.291(2)	65 nm CMOS
[33]	QVCO	90-94	4	43.2	-110.5(1)	173.5	n.a.	n.a.	n.a.	65 nm CMOS
This work	**QVCO**	**71.4-76.1 / 85.6-90.7**	**9.8**	**35.6**	**-114.2/-117.7 / -107/-110**	**176.3/179.4 / 170.2/173.4**	**191.4/194.5 / 185.3/188.5**	**<1.5° / <3.5°**	**0.031**	**28 nm CMOS**

(1)Estimated from the reported PN @1 MHz offset. (2)Graphically estimated.

of total tuning range. By varying the A-MOS varactor voltage from 0 V to 1.2 V and acting on the 2 binary-weighted digitally controlled MOM capacitors, the oscillator realizes continuous tuning within the two bands.

Fig.16(a) and Fig.16(b) show the measured phase noise from a 72.7 GHz and 88.2 GHz carrier respectively. The signal is measured at the output of the buffer directly at mm-Wave and downconverted with an external mixer. The prototype achieves a measured phase noise at 1 MHz and 10 MHz offset of -93.5 dBc/Hz and -117.7 dBc/Hz from a 72.7 GHz carrier and -86.2 dBc/Hz and -110 dBc/Hz from a 88.2 GHz carrier. The measured $1/f^3$ corner is $\sim$2 MHz. The same measurements are repeated over the tuning range are summarized and compared against simulations in Fig.17(a) at 10 MHz offset, showing that the measured phase noise ranges from -114.2 dBc/Hz to -117.7 dBc/Hz in the lower band and from -107 dBc/Hz to -110 dBc/Hz in the higher one. The resulting measured noise figure of merit ranges from 176.3 dBc/Hz to 179.4 dBc/Hz and from 170.2 dBc/Hz to 173.4 dBc/Hz in the higher and lower band respectively, as reported in Fig.17(b) together with the expected results. No RF transistor model was available during the design phase, resulting in an inaccurate estimation of the ON resistance of M_{SW}, much larger than the other transistors by design as explained in Section III. The measured oscillation frequency in the higher band shows therefore a shift of about 4.6 GHz toward higher frequencies, giving rise to a deviation from the optimal design point and a degradation of phase noise performance in this band.

To measure the quadrature amplitude and phase imbalance, an external mm-Wave signal is applied to the on-chip I/Q mixer driven by the QVCO. The resulting downconverted IF outputs are then measured with a sampling oscilloscope and shown in Fig.18. Measurements repeated over the whole tuning range prove a phase error less than 1.5° in the lower band and less than 3.5° in the higher one. The amplitude error stays always below 1 dB in both bands. Noteworthy, in a practical system relatively simple on-chip calibration techniques may be adopted to compensate for such a limited phase error, allowing high order modulation schemes as 64-QAM [4].

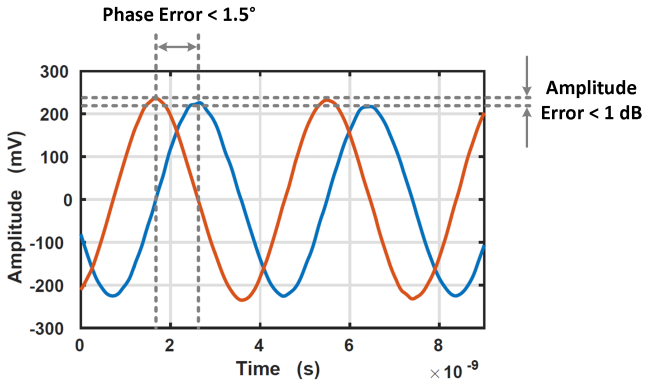

Fig. 18. Measured phase and amplitude imbalance of the I/Q signals downconverted to 260 MHz.

Table I summarizes and compares the measured performance of the quadrature VCO prototype to state-of-the-art integrated quadrature frequency generation circuits in the 70 GHz to 100 GHz band. Benefited by the presented design techniques, this work achieves the lowerst power consumption while occupying the smaller silicon area, and showing a better or comparable phase noise that varies less than 3.5 dB within each band. To compare different designs, we adopt two noise figure of merits defined as [11], [34]

$$FOM = 10log_{10}\left[\left(\frac{f_o}{\Delta f}\right)^2 \frac{1}{PN(\Delta f)P_{DC}}\right] \quad (24)$$

$$FOM_A = 10log_{10}\left[\left(\frac{f_o}{\Delta f}\right)^2 \frac{1}{PN(\Delta f)P_{DC}Area}\right] \quad (25)$$

where f_o is the oscillation frequency, Δf is the frequency offset from the carrier, P_{DC} is the dc power consumption expressed in mW and $Area$ is expressed in mm^2.

When such quadrature generation circuits are employed in direct conversion transceivers, the LO feedthrough and PA pulling may become serious issues [4], [35]–[37]. It is therefore desirable to keep the number of on-chip inductors

as small as possible and, in mm-Wave CMOS design, area serves as straightforward measure of this. Among the excellent designs in Table I, this work stands out for the lowest reported silicon area, without trading in power consumption or phase noise performance, leading to a measured FOM$_A$ between 3.6 dB and 12.8 dB higher than the best previously reported one.

V. Conclusion

A fundamental E-Band quadrature VCO based on gate-to-drain transformers to realize accurate quadrature phases and switched coupled inductors for tuning extension has been presented and analyzed. An in depth discussion of the phase noise mechanism, adopted tuning extension technique and phase error under tank mismatch has been reported, leading to optimal design for minimum phase noise and minimum phase error at the same time. Layout and implementation details relevant for mm-Wave oscillators implemented in deep-scaled CMOS technology have been addressed. The QVCO prototype is tunable from 71.4 GHz to 76.1 GHz in the lower band and from 85.6 GHz to 90.7 GHz in the higher one, and shows low measured phase noise performance without trading in silicon area. The resulting FOM$_A$ across the tuning range advances the state-of-the-art between by 3.6 dB and 12.8 dB.

Appendix

Assuming differential quadrature operation, the equivalent ac large signal model of the circuit schematic in Fig.1 can be redrawn as in Fig.19, where the ground reference is instrumentally shifted. Following the dissertation presented by Bevilacqua and Andreani in [38], in steady state is now possible to replace the transconductor with its describing function approximation [18]. The resulting circuit is shown in Fig.20. By applying the Norton's theorem the current source $I_{\omega 0}$ can be substituted with an equivalent current source $\beta I_{\omega 0}$ in parallel with C_m as in Fig.4, given

$$\beta = \frac{(sC_1 - jY_{12} + Y_{22})C_2 + C_1 Y_{22}}{(sC_1 + 2Y_{22})C_2 + C_1 Y_{22}} \qquad \text{(A.1)}$$

Since β is in general a complex number (i.e. the current flowing through the transistor $I_{\omega 0}$ and $\beta I_{\omega 0}$ are not in phase) and the transistor does enter the triode region as discussed in Session II-D, the general result on phase noise stated in [39] and [25] does not apply. Therefore, in this work this simplified model is only used to get insight into the quadrature operation of the circuit and obtain an approximated expression of the oscillation frequency.

Acknowledgment

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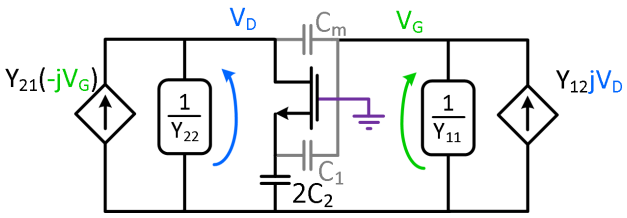

Fig. 19. Single ended AC large signal equivalent half circuit of the oscillator with an instrumental shift of the reference ground plane.

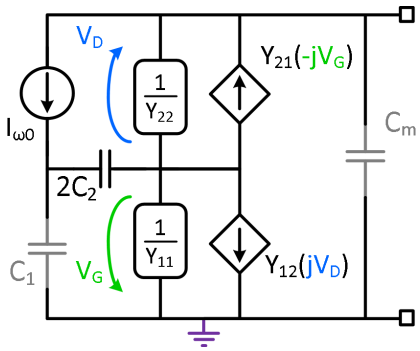

Fig. 20. Rearrangement of the circuit in Fig.19 where the transconductor is replaced with its describing function approximation.

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